Final Report - 1913996
Validation of Ambient Thermal Electric Conversion

1. Summary

Overview

One of the lessons of this project is how to better describe our work:

> There are two main pieces to our project. The first piece is the underlying physics, where we find semiconductors under specific conditions result in two different temperatures at the same location. The second piece is an engineered heat engine (Peltier Effect), which exploits this temperature difference.

Validity of ATEC structure for direct conversion of ambient heat to electricity rests on the fact of flow of carriers (electrons) from higher densities of state to lower densities of state. The Yang model for heterojunctions predicts such carrier flows. In this work, two proofs were pursued to validate the ATEC model:

- Measurements on LED spectrum that might show evidence in photo-emissions at zero bias.
- Voltage measurements across prototype ATECs that might confirm their model (which is based on the Yang model)

In support of this, there were four major goals:

- Verification of LED evidence showing Yang-predicted carrier flows.
- Authentication of our work on ambient thermal electric conversion (ATEC) by a recognized expert in semiconductor physics.
- Fabrication of a prototype ATEC device of HgCdTe and measurement of device performance.
- Modification of commercialization plan to reflect learnings about the market.

NSF asked us to engage a recognized expert in semiconductor physics to authenticate our development work on ambient thermal electric conversion. We asked Dr. Matt Graham of Oregon State University Department of Physics, who has 34 relevant published papers (as of 4/2019), to assist with this. He:

- Reviewed the Yang paper describing carrier movement across semiconductor heterojunctions (which underpins the models we used for ATEC). A Silvaco technical representative averred that the Yang model is indeed used in current versions of Silvaco's modeling software.
- Walked through the ATEC model outputs for both AlGaAs and HgCdTe, and noted that both showed higher voltages than were measured from prototypes.
- Oversaw extensive lab work setup and processes to measure LED behaviour near zero bias. The measurements confirm that photo-recombination continues to exist at and below zero bias. The measurements further showed that "hot electrons" in the LED active region have a temperature more than 100 ^{o}C higher than their lattice. The electron flow is predicted by Yang while "hot electrons" seem like straight-forward kinetics. We did not expect to find this self-establishing temperature difference when we

started exploring LEDs. We plan to publish a paper on these results with Dr. Graham, our Technical Advisor from Oregon State University.

LED Behavior

For LEDs, we want to show that movement of carriers across heterojunction are consistent with Yang model, upon which ATEC is designed

For LEDs, the measurements confirm that photo-recombination continues to exist at and below zero bias (see Products/ Appendix 1 - LED Tests/ Figure 7. Semilog plot of 1650nm LED intensity).

Temperature measurements from LEDs (from bulk material per environment and from electrons in the active region from photoemission spectrum) indicate distinctly different temperatures coexisting in the same body. “hot electrons” in the LED active region have a temperature 150 ^{o}C higher than their lattice (see Products/ Appendix 1 - LED Tests/ Figure 12. Implied temperature against applied voltage). With sufficient negative bias across LED, blackbody radiation stops. The electron flow is predicted by Yang, while “hot electrons” seem like straight-forward kinetics. We did not expect to find this self-establishing temperature difference when we started exploring LEDs. It has apparently not been previously reported.

HgCdTe Prototypes

Our NSF grant supported fabrication of a first prototype of HgCdTe. We engaged EPIR Technology to build a prototype ATEC with specifications per Table 1 of Appendix 2. EPIR took nearly three months to develop and verify fabrication steps, and another month for growth of an array of 36 devices, and completing etching and metallizing 6 of them (see Appendix 2). Each mesa measured 2 mm square and about 6 microns thick. We recorded voltages from five of the devices:

1 1.7 uV	2 2.3 uV	3 2.4 uV
4 N/A	5 5.2 uV	6 2.8 uV

These measurements were made from top contact, through top contact layer, HgCdTe mesa and bottom contact layer, and finally bottom contact (see Appendix 2 - HgCdTe ATEC Tests for other point-to-point measurements).

These measured voltages were much lower than we would have liked, but we know some of the reasons for this. Largely because of budget limits, we:

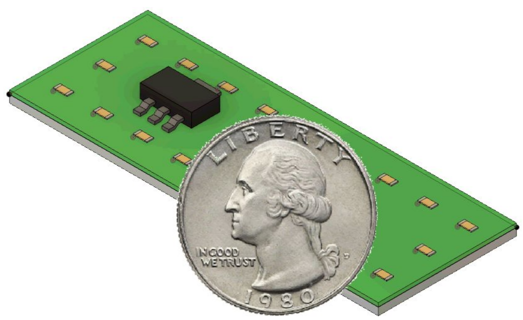
- Asked EPIR to omit the p-doped layers
- Changed doping specification to 10^{16}, rather than 10^{18}

Voltage was also low because semiconductor structures - especially HgCdTe - have high surface flows at the edges between layers, thus leaking off the current down the mesa sides instead of the higher-impedance core, reducing the measurable voltage. We did not ask for passivation which is commonly used to block such flow. We had an equivalent problem in AlGaAs - solved by multiple etchings at the edge - which improved device performance about two fold.

A non-technical result of this work is that we have developed a comfortable working relationship with EPIR, trusting both their skills and their earnestness. Further, EPIR is well prepared to improve future prototypes.

<u>Commercialization Plan</u>
Our original plan was to approach the smartphone manufacturers. Our survey of end users showed enthusiasm for a smartphone battery replacement at cost $100. But our outreach to about 30 personal electronics manufacturers drew no interest. So we can fulfill a market want, but need a lower-threshold entry point.

Pushed by Boot Camp and assisted by Dawnbreaker, we pivoted our Commercialization Plan away from marketing battery replacements to personal electronics makers and toward engaging electronic parts suppliers to make small power supply units for remote sensing. In our conversations at Boot Camp, we found several companies that were very interested in a 0.1 W unit for $100. For remote sensing applications, power requirements are often small, while the cost of reliable power can be high.

	
Figure 1. Initial package will use industry-standard form 0603 (1.8 mm by 0.9 mm, as shown on a dime).	**Figure 2.** The 0603 form is easily incorporated in electronics assemblies such as this for smartphone power supply, with: heat transfer/mechanical base (gray), PC board (green), ATEC in 0603 (yellow), voltage regulator (black). Multiple small parts are used to aid heat conduction. They are connected in series to develop required voltage. The black element is a voltage regulator.

The semiconductor structure will be used as a power supply for a range of devices. There are four main steps to do this:

- Fabrication of layers of the structure on silicon wafers using standard equipment and techniques. Each spot will be built with perhaps hundreds of cycles of the structure to generate voltages needed.
- The wafer is then diced into individual devices that produce requisite voltage and of sufficient area to generate required current (and thus required power)
- The devices are individually packed into industry-standard 0603 form (see Figure 3-1).
- Devices as needed for use are placed on a board and further packaged as needed for specific applications (see Figure 3-2).

We looked at processes needed to fabricate ATEC power supplies using industry-standard technology and companies where practical. We computed a cost to produce a phone power supply as less than $0.50.

2. Problems and Resolutions

We encountered a number of problems along the way to making reliable measurements on LEDs and prototype ATECs. None was pivotal, and we believe we have solutions, but implementation was beyond our budget.

Solved problems included:

- Fabricators were initially reluctant to engage in this work. Before completing our proposal to NSF, we traveled to meet with a fabricator to exchange information about our needs and their capabilities. This turned out to be a critical step, as we were able to persuade them of the merits of our physics and thus involve them in looking seriously at fabrication issues.
- Potential fabricators were unable to dope to modelled level, so we reduced the doping requirement (at corresponding risk to performance).
- Our initial measurements of ATEC output showed an AC component (noise) near to the DC component (signal). We reduced noise through filtering by the amplifier, and by using battery power for amplifier and voltmeter, and by opto-isolation. We also reduced thermal variations from room air currents by adding a foil hood.

3. Unresolved Problems and Unfilled Research Objectives

Our work with LEDs is not yet complete, though we expect to be able to complete that within our current resources.

There are a number of pending problems we encountered with ATEC prototypes. We have plans for resolution in future prototypes. Solutions depend on budget and fabrication considerations.

- Lower contact impedance is high (10-20 ohms).
- Mesa edge impedance appears to be low (less than 1 ohm, possibly micro-ohms).
- Structure impedance may be low. We have no means to accurately measure this.
- Our best measurements only show a lower bound on device performance.

- Indium-Gold contacts are difficult to bond to. The challenge is that Indium melts at 180 C, while thin layers of gold are easily torn. EPIR says they have the skill and correct wire-bonding equipment.

There are two areas for which we need solutions to bring ATEC fabrication costs down sufficiently to serve the full potential market.

HgCdTe prototypes performance is not yet good enough to serve the market for remote devices, except for extreme edges of the market. Based on experience of EPIR, we are probably seeing high leakage currents at the mesa sides. We will need to explore the use of passivation methods to block the leakage. We should also explore optimization of Hg-Cd content, alternative material sets such as InGaAs and InGaSb, and use of the p-doped layers, and doping levels. InGaAs and InGaSb are more widely used in semiconductor fabrications, but are three to six orders less effective. Finally, we should identify the cause of unexpectedly high voltage between bottom contact and etched region just to make sure we are not missing something useful.

We also need to engineer the devices to reduce production costs. We could redesign the method for creating bottom contact to avoid etching mesa to separate it from the bottom contact layer. We could also evaluate lateral design production issues of alignment and material-switching process.

4. Conclusions

The measurements on ATEC prototypes showed voltages that were different among them but consistent and persistent for each device (see Appendix 2). While there was of course measurement noise, it appeared to be below well the level of signal. The differences among devices pretty well exclude biases. Our conclusion: the devices self-create a harvestable voltage, a result well worth pursuing.

Measurements on LEDs show that semiconductors operate in a domain that does not fully adhere to conventional thermodynamics. Our interpretation follows: For carriers in semiconductors, ‘space’ is not ‘flat’ or uniform. It is similar to the distortion due to gravity, but it is not smooth or uniformly curved. Statistics which assume a flat, uniform space are therefore not necessarily valid, and alternate results might be possible. The LED results seem to bear this out, and warrant further investigation in their own right.

The next steps we have identified should each move the ATEC to higher performance. We are also working with Dr. Graham towards a paper on the subject of two temperatures in LEDs.

Appendix 1 - LED Tests

Abstract

This study provides a proof-of-concept prototype of an Indium-Gallium-Arsenide (InGaAs) LED which shows low level energy production using ambient heat that could be harvested for commercial purposes. Our objective is to replicate and expand on recent measurements showing that semiconductor carriers at equilibrium can have an electronic temperature higher than the lattice temperature. This will ultimately help validate commercial viability of a potential ambient thermal electric converter for low cost energy production.

Theory

This experiment investigated the validity of the two different behavioral models showcased in these equations [3].

Schroeder Model:

$$J_{n,p} = -q[v_{n2,p2}T_{n2,p2}(n,p)_2 - \left(\frac{m_{n2,p2}}{m_{n1,p1}}\right) v_{n1,p1}T_{n1,p1}(n,p)_1 e^{\left(\frac{-\Delta W_c}{k_B T_{n1,p1}}\right)}]$$

Yang Model:

$$J_{n,p} = -q[(1+\sigma_{n,p})v_{n2,p2}T_{n2,p2}(n,p)_2 - (1+\sigma_{n,p})\, v_{n1,p1}T_{n1,p1}(n,p)_1]\; e^{\left(\frac{-\Delta W_C}{k_B T_{n1,p1}}\right)}$$

The most significant difference between the two is the ratio of masses term in the center of Schroeder. This term means that for any junction where the Fermi level is uniform across the junction (implying no voltage), there will be no flow of holes or electrons. Yang implies that any change in the density of states (N_c or N_v) produces a current for one or both carriers even when the Fermi levels are aligned. Stopping that current would require charge build-up and/or a temperature difference.

The second difference is the tunneling term (1+ $\sigma_{n,p}$). This term is 1 unless there is charge buildup or depletion.

Appendix 1 - LED Tests

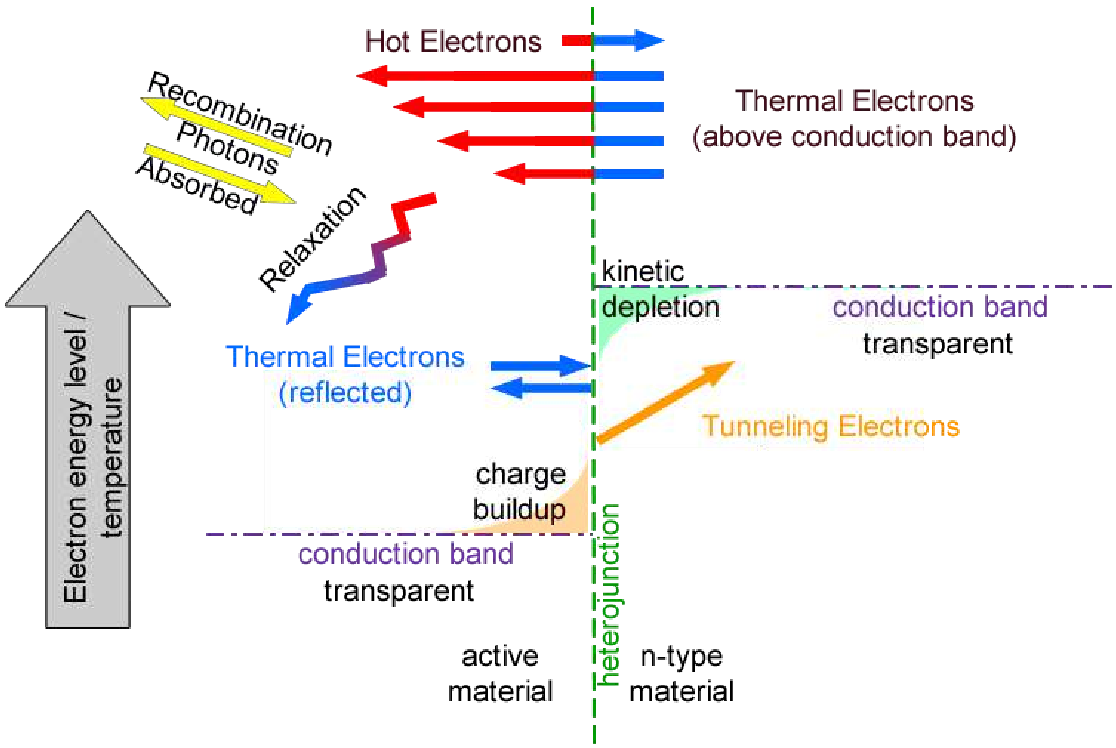


Figure 1. Relevant Paths for Electrons at the n-type heterojunction of a LED. Note that electrons crossing right to left will initially be at least ΔE_g above the conduction band ('Hot Electrons') and will relax down toward a Fermi-Dirac distribution through collisions.

Figure 1 represents electron activity around the n-type heterojunction of a double-heterojunction LED. The two materials have different band gaps and work functions, resulting in a conduction band mismatch. When an electron moves across the heterojunction, the energy must either go to or come from somewhere. We show this in terms of electrons retaining the same energy relative to vacuum on either side of the junction. An electron which had been at the conduction band on the right side would therefore be far above the band on the left, having an energy of ΔE_g.

Under forward bias, some thermal electrons drift/diffuse into the active region and become Hot Electrons. This results in a significant excess of hot electrons. They may undergo some relaxation, including down to thermal levels. Some of these electrons will recombine with a hole, emitting a photon. Some hot electrons will scatter and diffuse back across the junction, again becoming thermal electrons. Some thermal electrons will tunnel and diffuse across the junction. The net result is a recombination temperature which is higher than the junction temperature.

Under reverse bias, drift is in the opposite direction. In this case, the high energy electrons freely drift from the active region into the supporting n-type material. For lower energy electrons, the probability of tunneling is a direct function of the electron energy. The net result is a recombination temperature which is lower than the junction temperature.

What we find is that even at zero volts, the emitted spectrum indicates an elevated temperature. That implies that hot electrons are still diffusing from right to left, and finding some alternate (tunneling) path to the right. This would be consistent with Yang, but not with Schroeder.

Experimental Setup

Figures 2 show the housing for the test target LED.

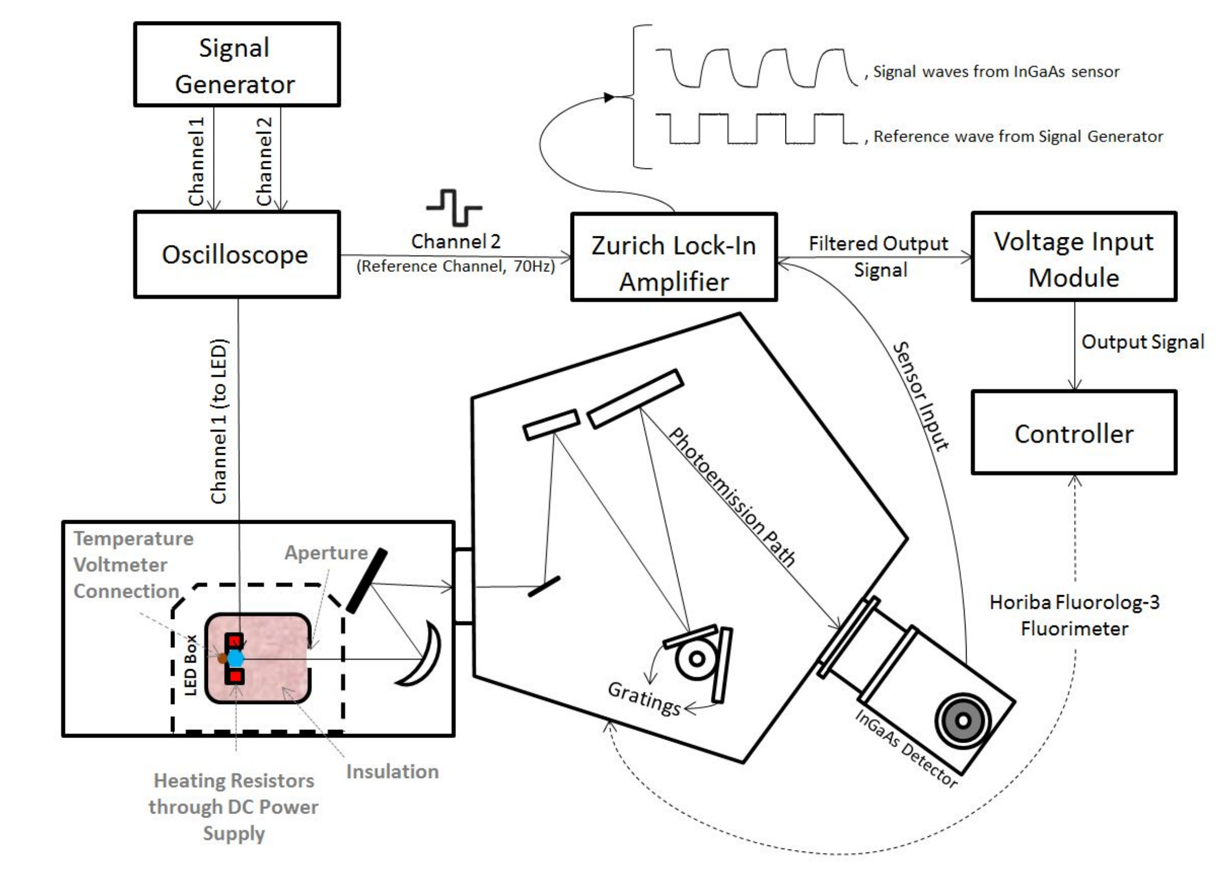
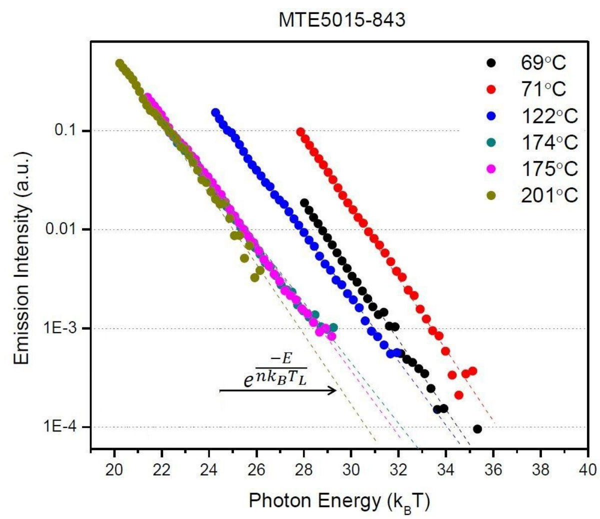


Figure 2. A schematic of the experimental set-up, including the LED box, showcasing the flow of input to output as well as the emission path of photons from the LED to the detector.

Appendix 1 - LED Tests

Results and Discussion

1. Experimental measurements of the emission spectrum of the InGaAs LED show a trend of increase in emission intensity as the electronic temperature increases. This trend is observed in both LEDs.



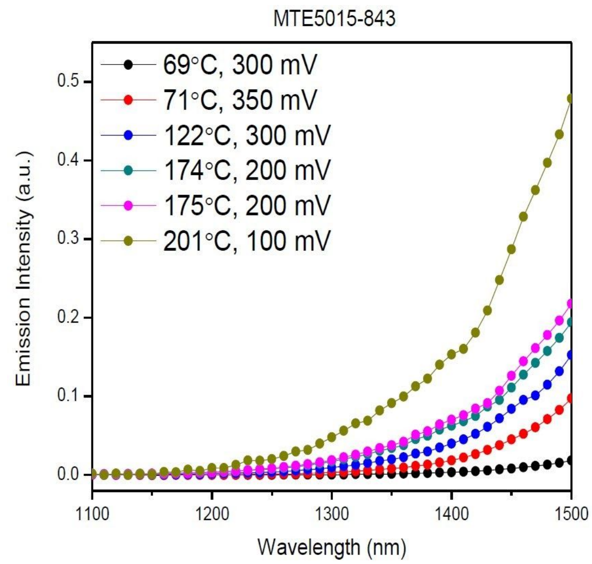


Figure 3. Emission spectrum of 1550 nm LED (MTE5015-843) against photon energy as a multiple of k_BT, plotted with vertical log scale. In the left graph, different vertical offsets are the result of different LED intensity. Horizontal offsets are the result of different operating temperatures.

2. Data taken can be further processed to calculate for the effective recombination temperature T_C. We used the following formula:

$$r(h\nu) = Ah\nu \,\mathrm{Re}\, \sqrt{h\nu - E_g}\, \exp\left(-\frac{h\nu}{k_B T_c}\right), \qquad (2)$$

The source paper by Vaitonis et al.[4] attributed the radiated temperature to heating within the device, which is reasonable for a high powered LED. We calculate that in our tested device, there was a maximum rise of 4 °C. The devices fail permanently at roughly 220 °C.

Appendix 1 - LED Tests

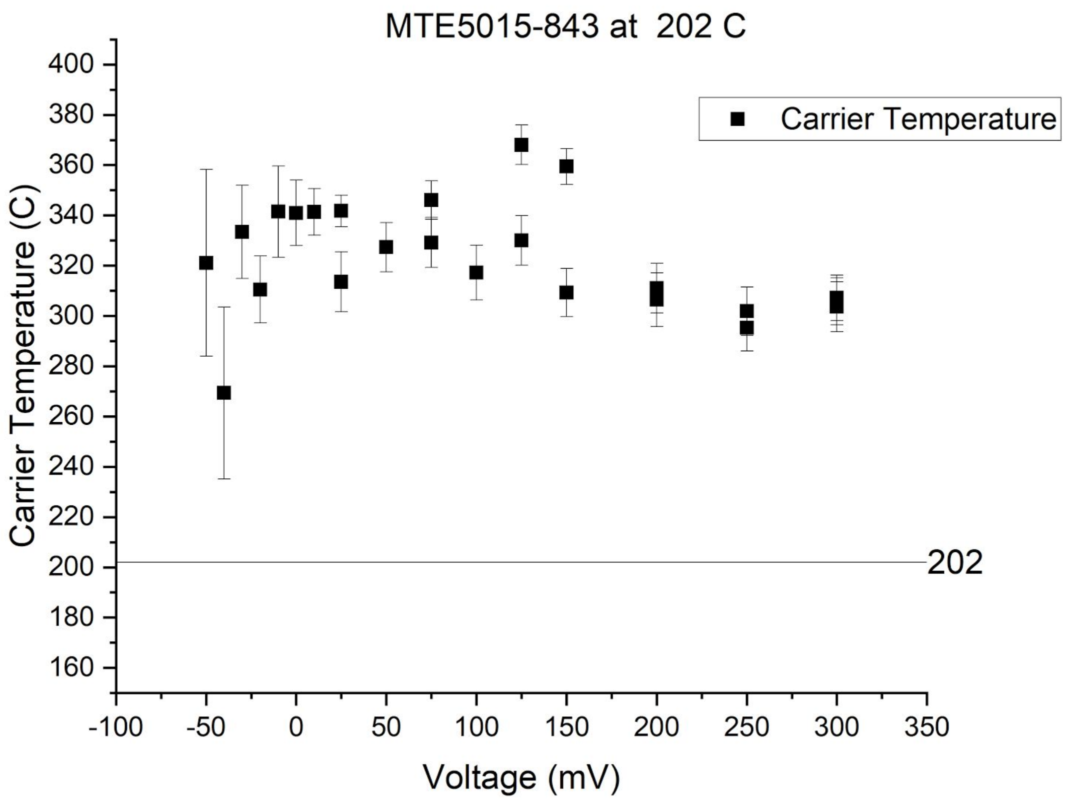


Figure 4. Electron temperature against applied voltage at 202°C. Data appear to preclude a uniform temperature within the device, even at zero bias.

This provided insight on the recombination temperature at close to 0 bias for the low-bandgap LED, which has shown to have an average above the lattice temperature.

Conclusion

The data collected experimentally as well as arithmetically appears to indicate a recombination (electronic) temperature which is different from the lattice temperature, even at zero bias.

References

1. Orem, Peter, Orem, Frank, “Implementing Demons and Ratchets”, *Entropy* 19(1):34, January 2017, DOI:10.3390/e19010034

2. Orem, Peter, et al. “Measuring Thermally-Driven LED Emissions via Voltage Modulation near Zero Bias.” *Electronics*, vol. 7, no. 12, 2018, p. 360., doi:10.3390/electronics7120360.

3. Yang, Kyounghoon, et al., “Numerical Modeling of Abrupt Heterojunctions Using a Thermionic-Field Emission Boundary Condition.” *Solid-State Electronics*, vol. 36, no. 3, 1993, pp. 321–330., doi:10.1016/0038-1101(93)90083-3.

4. Z. Vaitonis, P. Vitta, A. Žukauskas, “Measurement of the junction temperature in high-power light-emitting diodes from the high-energy wing of the electroluminescence band”, Journal of Applied Physics, 103(9):093110, May 2008, DOI: 10.1063/1.2908176.

Appendix 2 - HgCdTe ATEC Tests

Test Purpose: to determine if the ATEC prototypes of HgCdTe as specified by ThermaWatts and fabricated by EPIR Technology produce a reliably measurable voltage.

Test Targets
EPIR delivered an assembly of three full and three half (cut) devices, for a total six devices to test. Each device is configured as shown in Figures 1a and 1b. Note the size indicated. Figures 1a and 1b are images of an array of devices and a single device. Table 1 lists the layers in the growth, totaling 7.430 µm. EPIR spent about two months testing their techniques for layer deposition.

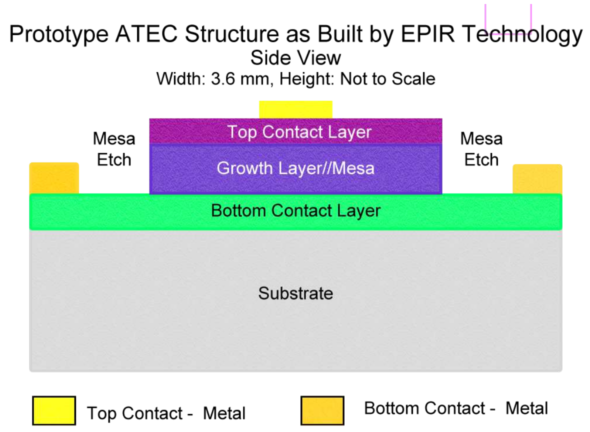


Figure 1a. Top and bottom contacts are Indium/Gold, top and bottom contact layers are 3 µm of n-doped HgCdTe, growth Layer is ATEC structure, which totals 8 µm deep.

Figure 1b. Mesa and Top Contact Layer were etched down to the level of the bottom contact layer. The Growth Layer is covered by the Top Contact Layer.

Test Environment
Pertinent characteristics of the test environment were:

- The room is unheated. Air is drawn from leakage at its inside door. There is some heating/cooling at covered windows. An exhaust hood is nearly sealed, reducing air drawn under the inside door.
- The test bed is 60 cm x 40 cm x 1 cm steel platform
- The test target is mostly under hood to limit air currents
- The room lighting is off. There is low lighting from the exhaust hood several feet away from the test bed, and from a computer monitor.

Appendix 2 - HgCdTe ATEC Tests

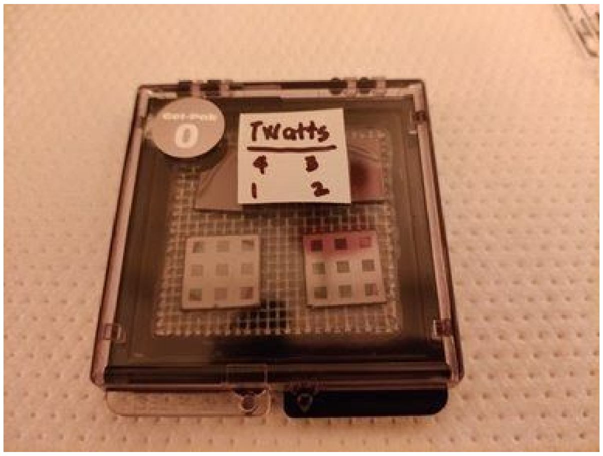


Figure 2a. Picture of two 3 x 3 assemblies of ATEC prototype devices.

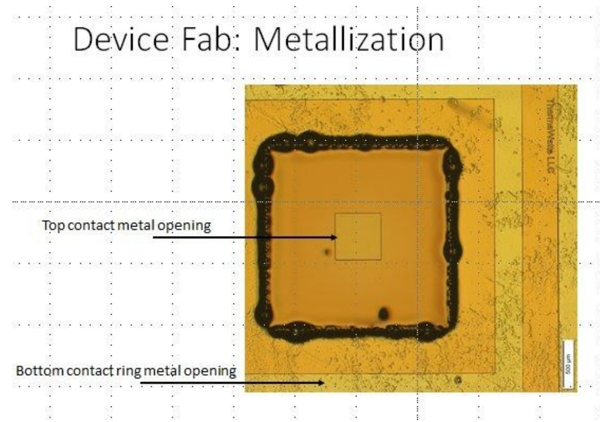


Figure 2b. Picture of prototype ATEC device after mesa etch (irregular black area) and metallization of the contact areas (light square in center, light box near outer edges).

Table 1 - Layer configuration for ATEC Prototypes

#	% Cd	Thick*	Dope	Conc**		#	% Cd	Thick*	Dope	Conc**
Btm	0.3	3.000	n	2		12	0.3	0.035	n	2
1	0.3	0.430	n	1		13	0.3	0.430	n	1
2	0.3	0.025				14	0.3	0.025		
3	0.2	0.025				15	0.2	0.025		
4	0.2	0.200	n	1		16	0.2	0.200	n	1
5	0.2	0.035	n	2		17	0.2	0.035	n	2
6	0.3	0.035	n	2		18	0.3	0.035	n	2
7	0.3	0.430	n	1		19	0.3	0.430	n	1
8	0.3	0.025				20	0.3	0.025		
9	0.2	0.025				21	0.2	0.025		
10	0.2	0.200	n	1		22	0.2	0.200	n	1
11	0.2	0.035	n	2		Top	0.2	1.500	n	2
Total								7.430		

* Thickness in μm
** Scale by 1 E+16

Measurement Error Mitigation We have taken precautions against measurement error as described below:

<u>Meter bias</u>

- Shorted leads showed near-zero after amplification (see Shorted graph in Results of Tests on 12/26/19 from HgCdTe Prototypes Fabricated by EPIR, below)

<u>Thermoelectric (Seebeck) effect</u>

- Environment is controlled to limit effect of temperature gradient across test components

Appendix 2 - HgCdTe ATEC Tests

- Test target is small, about 2 mm between upper and lower contacts horizontally, and ~5 µm vertically.
- Test leads from amplifier and voltmeter and shorted at upper or lower contact show < 2 microvolt (<2 millivolts after amplification)

Induced from ElectroMagnetic Interference

- Limited noise source
    - Overhead lighting off
    - No air conditioning motors in the room
    - Foil hood over test target and probes leads
    - Meter leads shielded
- When reversing probes, the voltage follows the part orientation.

Capacitance

- The device structure is similar to a capacitor, with two conductive layers sandwiching a low-conductance layer.
    - We considered that the device could have capacitance no greater than a Tantalum capacitor with the same footprint as our device, which could be 100 uF.
    - The measured resistance of the six devices in hand was 15 to 20 ohms.
    - Computed time constant for capacitance of 100uF with internal resistance of 15 to 20 ohms is 1.5-2.0 milliseconds. Sample times ran to minutes.
- There may be other sources of capacitance in the test jig.
    - Shorting the test probes across a contact layer produced measurements of less than 2 uV (see Shorted graph in Shorted graph in Results of Tests on 12/26/19 from HgCdTe Prototypes Fabricated by EPIR, below).

Summary of Measurement Results

Table 2 shows approximate voltages as measured and then amplified by 1000 .Details of test results are shown in Results of Tests on 12/26/19 from HgCdTe Prototypes Fabricated by EPIR.

Table 2. Approximate measured and amplified voltage from prototypes.

#	Voltage		#	Voltage		#	Voltage
1	1.7 mV		2	2.3 mV		3	2.4 mV
4	N/A		5	5.2 mV		6	2.8 mV

Appendix 2 - HgCdTe ATEC Tests

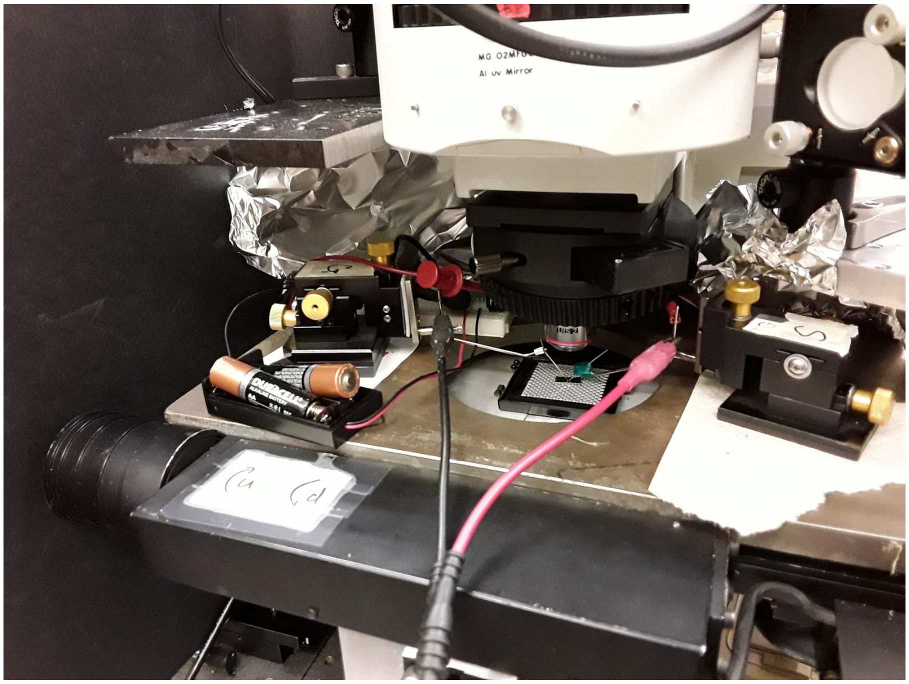


Figure 3. Image of Test Jig. The target is just right and below center, with tungsten probes on left and right. Amplifier is on white prototyping board just above the left probe. Left probe is attached to the amplifier. Both black and red leads are shielded. AA cells power the amplifier. Foil (upper half) partially cloak target from air currents and EMI.